
SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

FORM 8-K/A

CURRENT REPORT

Pursuant to Section 13 or 15(d) of
the Securities Exchange Act of 1934

January 18, 2002

Date of Report (Date of earliest event reported)

LATTICE SEMICONDUCTOR CORPORATION

(Exact name of registrant as specified in its charter)

Delaware

(State or other jurisdiction of
incorporation)

000-18032

(Commission File Number)

93-0835214

(I.R.S. Employer
Identification No.)

5555 NE Moore Court
Hillsboro, OR 97124-6421

(Address of principal executive offices)

(503) 268-8000

(Registrant's telephone number, including area code)

AMENDMENT NO. 2

The undersigned Registrant hereby amends Item 7 of its Current Report on Form 8-K, originally filed with the Securities Exchange Commission on February 4, 2002 and amended on April 2, 2002, reporting the acquisition by Registrant from Agere Systems Inc., a Delaware Corporation, of the field programmable gate array business of Agere, as set forth in the pages attached hereto.

Item 7. Financial Statements and Exhibits

(a) Financial statements of businesses acquired.

The required financial statements of the business acquired are set forth below.

FPGA Business of Agere Systems Inc.

Index to Financial Statements

For the year ended September 30, 2001

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Report of Independent Accountants

To the Board of Directors and Stockholders of
Agere Systems Inc.:

We have audited the accompanying statement of assets to be sold of the field-programmable gate array business ("FPGA") of Agere Systems Inc. ("Agere") as of September 30, 2001, and the related statement of net sales, cost of sales and direct operating expenses for the year then ended. These financial statements are the responsibility of Agere's management. Our responsibility is to express an opinion on these financial statements based on our audit.

We conducted our audit in accordance with auditing standards generally accepted in the United States of America. Those standards require that we plan and perform the audit to obtain reasonable assurance about whether the financial statements are free of material misstatement. An audit includes examining, on a test basis, evidence supporting the amounts and disclosures in the financial statements. An audit also includes assessing the accounting principles used and significant estimates made by management, as well as evaluating the overall financial statement presentation. We believe that our audit provides a reasonable basis for our opinion.

The accompanying financial statements were prepared for the purpose of complying with the rules and regulations of the Securities and Exchange Commission (for inclusion in the current report on Form 8-K of Lattice Semiconductor Corporation) and, as described in Note 1, are not intended to be a complete presentation of FPGA's financial position, results of operations and cash flows.

In our opinion, the financial statements referred to above present fairly, in all material respects, the assets to be sold of FPGA as of September 30, 2001 and the net sales, cost of sales and direct operating expenses described in Note 1 of FPGA for the year then ended in conformity with accounting principles generally accepted in the United States of America.

As discussed in Note 2, the financial statements have been revised to include an allocation of expenses related to Agere's global sales force.

/s/ PRICEWATERHOUSECOOPERS LLP

Florham Park, New Jersey

March 7, 2002, except as to the
matter described in Note 2, as to
which the date is November 21, 2002

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Agere Systems Inc.

FPGA Business

Statement of Assets to be Sold (See Note 1)

As of September 30, 2001

(In thousands)

Inventories	\$	7,124
Servers, work stations and laboratory equipment		<u>758</u>
Total assets to be sold	\$	<u>7,882</u>

The accompanying notes are an integral part of these financial statements.

Agere Systems Inc.

FPGA Business

Statement of Net Sales, Cost of Sales and Direct Operating Expenses
For the Year Ended September 30, 2001 - Revised
(in thousands)

Net sales (includes \$44,543 to Lucent Technologies, Inc.)	\$	68,987
Cost of sales		<u>55,546</u>
Gross profit		<u>13,441</u>
Direct operating expenses		
Research and development		15,454
Marketing and sales		<u>5,270</u>
Total direct operating expenses		<u>20,724</u>
Excess of cost of sales and direct operating expenses over net sales	\$	<u>(7,283)</u>

The accompanying notes are an integral part of these financial statements.

Agere Systems Inc.

FPGA Business

Notes to Financial Statements
(In thousands)

1. Background and Basis of Presentation

The accompanying financial statements have been prepared for the purpose of presenting the net assets of the field-programmable gate array business ("FPGA") of Agere Systems Inc. ("Agere") which were sold pursuant to the purchase and sale agreement dated December 7, 2001, between Agere and Lattice Semiconductor Corporation ("Lattice") and its net sales, cost of sales and direct operating expenses. The financial statements do not reflect any effects of the sale of the business. The sale of the net assets for \$250,000 in cash was completed on January 18, 2002. As part of the sale, approximately 100 employees were transferred to Lattice. FPGA represents a product family managed as part of Agere's Integrated Circuits segment consisting of its general-purpose ORCA™ field-programmable gate array products, field-programmable system on a chip products and related software design tools. Prior to Agere's separation from Lucent Technologies Inc. ("Lucent") effective February 1, 2001 (the "Separation"), FPGA was managed as part of Lucent's Microelectronics and Communications Technologies segment. Management does not analyze FPGA as a separate line of business.

Agere did not maintain FPGA as a separate business unit and external financial statements historically have not been prepared. The accompanying financial statements have been derived from the historical records of Agere in order to present the assets to be sold of FPGA as of September 30,

2001 and the net sales, cost of sales and direct operating expenses for the year then ended in accordance with accounting principles generally accepted in the United States of America.

The statement of net sales, cost of sales and direct operating expenses for FPGA includes allocations for certain costs, including factory overhead and support functions, such as, quality assurance, logistics, and information technology, and the global sales force. There are certain costs that have not been allocated including basic research, corporate-wide marketing and sales, general and administrative expenses, interest and income taxes. Since FPGA was never a separate business unit, these costs relative to FPGA were not segregated for external financial reporting purposes. Accordingly, the inclusion of these charges is not practicable.

All cash flow requirements of FPGA were funded by Agere and, prior to the receipt by Agere of the proceeds from its initial public offering in April 2001, by Lucent. Therefore, a statement of cash flows, including cash flows from operating, investing and financing activities is not presented as FPGA did not maintain a cash balance. These statements are not intended to be a complete presentation of FPGA's financial position, results of operations and cash flows. The historical operating results of FPGA may not be indicative of its results in the future.

Agere provides FPGA with various infrastructure and support services, which among other things include real estate, computer and network systems, human resources, payroll, accounting and cash management and legal support. In addition, FPGA's sales are derived through the Agere sales force.

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Agere Systems Inc.

FPGA Business

Notes to Financial Statements
(In thousands)

2. Revision of Financial Statements

Marketing and sales expenses have been revised to include an allocation of the cost of Agere's global sales force, which sells all of Agere's Integrated Circuits segment products, including FPGA products. This revision resulted in a \$2,405 increase in marketing and sales expense for the year ended September 30, 2001 from the amount previously reported.

3. Summary of Significant Accounting Policies

Revenue Recognition

Revenue is generally recognized when all significant contractual obligations have been satisfied, title and risk of loss have been transferred to the customer and collection of the resulting receivable is reasonably assured. FPGA recognizes revenue from product sales to distributors when all obligations have been satisfied. Revenue from product sales is recognized at time of delivery and acceptance, and after consideration of all of the terms and conditions of the customer contract.

FPGA adopted as of October 1, 2000, Securities and Exchange Commission Staff Accounting Bulletin 101, "Revenue Recognition in Financial Statements" ("SAB 101"). SAB 101 provides guidance on the recognition, presentation and disclosure of revenue in financial statements. The impact of adoption was not material to the statement of assets to be sold and the statement of net sales, cost of sales and direct operating expenses.

Cost of Sales

Cost of sales includes direct manufacturing costs and allocated costs of approximately \$9,000 consisting of certain indirect factory overhead, including indirect labor and support functions such as quality assurance, factory accounting, logistics, information technology and such allocations are based on the percentage of FPGA planned revenue compared to total Integrated Circuits segment planned revenue.

Research and Development Expense

Research and development costs are charged to expense as incurred. Direct research and development expenses include salaries and benefit costs of FPGA personnel that conduct applied or development research to develop new products, technologies and software that are used in the design and manufacture of FPGA products.

Marketing and Sales Expense

Marketing and sales expense includes direct costs of product management, market planning, market operations, product line planning and management, advertising and an allocation of the salary, benefit, travel and other support costs related to Agere's global sales force based on the percentage of FPGA planned revenue to total Integrated Circuits segment planned revenue. Costs associated with Agere's corporate-wide advertising, business development, strategic planning and other indirect support activities were not allocated to FPGA.

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Inventories

Inventories are stated at the lower of cost, determined on a first-in, first-out basis, or market, and include any inventory located at distributors. Substantially all product located at distributors was returned subsequent to the sale of FPGA.

Inventories at September 30, 2001 consist of the following:

Work-in-process	\$	3,724
Finished goods		<u>3,400</u>
	<u>\$</u>	<u>7,124</u>

Raw materials have not been allocated to FPGA since they relate to common components for all integrated circuits and are not specifically identifiable to FPGA.

Servers, Work Stations, and Laboratory Equipment

Laboratory equipment consists of research and development and test equipment and is stated at cost less accumulated depreciation of \$1,048 at September 30, 2001. Depreciation is determined using the straight line method over estimated useful lives of 3 to 5 years. Depreciation expense for the year ended September 30, 2001 amounted to \$223.

Use of Estimates

The preparation of financial statements and related disclosures in conformity with generally accepted accounting principles requires management to make estimates and assumptions that affect the reported amounts of assets and liabilities and disclosure of contingent assets and liabilities at the date of the financial statements and revenues, costs and expenses during the period reported. Actual results could differ from those estimates.

4. Concentration of Net Sales

Lucent accounted for approximately 65% of net sales for the year ended September 30, 2001. The loss of this customer could have a material adverse effect on the statement of assets to be sold and the statement of net sales, cost of sales and direct operating expenses.

5. Employee Benefit Plans

FPGA participates in various employee benefit plans, including pension, savings, post-retirement and post-employment plans, which were sponsored by Lucent until January 1, 2002 when Agere took responsibility for all plans except the pension plan, which Lucent still maintains. Detailed information concerning costs of these plans is not available for FPGA but costs of these plans are included to the extent labor costs are included in the statement of net sales, cost of sales and direct operating expenses. The specific charges and obligations under these plans related to FPGA are not separately identifiable.

6. Leases

FPGA leases servers and work stations under agreements that expire in various years through 2004. Rental expense under operating leases was \$609 for the year ended September 30, 2001. The table below shows the future minimum lease payments under non-cancelable operating leases at September 30, 2001. Such payments total \$1,042.

Year Ending September 30,			
2002	2003	2004	Later Years
\$675	\$366	\$1	\$—

7. Manufacturing

FPGA's products have historically been manufactured at domestic and international Agere-owned facilities and third party foundries. Because the manufacturing operations are not separately identifiable to FPGA and were not sold, related manufacturing assets have been excluded from the accompanying statement of assets to be sold.

8. Sale of FPGA Business

In connection with the sale of FPGA, Agere and Lattice have entered into a Transition Services Agreement, a Sublease Agreement, a Wafer Foundry Agreement, a Wafer Probe, Package Assembly, Test, Mark and Pack Agreement, and an Intellectual Property Agreement.

Transition Services Agreement

Agere agreed to provide Lattice certain temporary transition services in order to continue the operations of FPGA. These transition services include product and package development, assembly and test engineering, quality assurance, tactical marketing, production control and scheduling, information technology and use of certain Agere facilities.

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Agere Systems, Inc.

FPGA Business

Notes to Financial Statements
(In thousands)

Sublease Agreement

Agere agreed to sublease to Lattice approximately 25,000 square feet of space at Agere's 12th Street Facility in Allentown, Pennsylvania, for a term ending on April 20, 2003.

Wafer Foundry Agreement

Agere agreed to manufacture and supply Lattice with semiconductor wafers for the field-programmable gate array products from Agere's Orlando wafer manufacturing facility.

Wafer Probe, Package Assembly, Test, Mark and Pack Agreement

Agere agreed to provide Lattice wafer probe, package assembly, test, mark and pack services for field-programmable gate array products.

Intellectual Property Agreement

Pursuant to an Intellectual Property Agreement, Lattice has also acquired certain intellectual property cores and patents that are unique to Agere's FPGA business. Additionally, the parties entered into a cross-license whereby Lattice received rights to Agere patents and certain intellectual property for use in current and future field-programmable gate array and field-programmable system on a chip products and Agere will continue to have access to the ORCA field-programmable gate array technology for incorporation into its "system-on-a-chip" integrated circuits.

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(b) Pro forma financial information.

The following unaudited pro forma condensed consolidated financial statements are presented for illustrative purposes only and do not purport to be indicative of the consolidated financial position or results of operations for future periods or the results that actually would have been realized had Lattice Semiconductor Corporation ("Lattice") and the FPGA Business of Agere Systems Inc. ("Agere") been a consolidated company during the specified periods. Further, non-recurring Purchase Accounting adjustments are excluded from the pro forma adjustments in the unaudited pro forma condensed Statement of Operations. The unaudited pro forma condensed consolidated financial statements, including the notes thereto, are qualified in their entirety by reference to, and should be read in conjunction with the historical consolidated financial statements and the notes thereto of Lattice which were previously reported in Lattice's Annual Report on Form 10-K for the year ended December 31, 2001, filed with the Securities and Exchange Commission, and the Agere financial statements and the notes thereto for the year ended September 30, 2001 included elsewhere in this Current Report on Form 8-K/A.

The following unaudited pro forma condensed consolidated financial statements are based on the respective historical audited consolidated financial statements and the notes thereto of Lattice and Agere after giving effect to the acquisition of Agere using the purchase method of accounting and the assumptions and adjustments described below. The purchase price was allocated to the estimated fair value of assets acquired and liabilities assumed. In performing the preliminary purchase price allocation, management considered various factors including an appraisal. The purchase price allocation is subject

to further refinement and change over the current quarters . Management is in the process of completing its plans related to the integration of Agere, and accordingly, the amounts recorded related to Agere are based on management's current estimate of those costs.

This Current Report on Form 8-K/A contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934.

The required pro forma unaudited financial information is set forth below.

PRO FORMA FINANCIAL INFORMATION
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LATTICE SEMICONDUCTOR CORPORATION
UNAUDITED PRO FORMA CONDENSED CONSOLIDATED BALANCE SHEET
September 30, 2001
(in thousands)

	Lattice	Agere FPGA	Pro Forma Adjustments		Pro Forma Combined
Current Assets:					
Cash and investments	\$ 540,120	\$	\$ (256,288)	A	\$ 283,832
Accounts receivable, net	19,251				19,251
Inventories	65,048	7,124	(4,552)	A	67,620
Prepaid expenses and other current assets	34,489				34,489
Deferred income taxes	35,588				35,588
	694,496	7,124			440,780
Intangible assets, net	227,105		230,915	A	458,020
Property and equipment, net	66,460	758	(524)	A	66,694
Foundry investments, advances and other assets	120,284				120,284
Deferred income taxes	74,493				74,493
	Total Assets	\$ 1,182,838	\$ 7,882		\$ 1,160,271
Current Liabilities:					
Accounts payable & other accrued exp.	\$ 32,346	\$	\$ 1,633	A	\$ 33,979
Accrued payroll obligations	19,741				19,741
Income taxes payable	1,348				1,348
Deferred income	23,342				23,342
	76,777				78,410
4¾% Convertible subordinated notes	260,000				260,000
Other long-term liabilities	17,848				17,848
Stockholders' equity:			(7,882)	A	
Stock and paid-in capital	546,939	7,882	7,014	D	553,953
Accum. other comprehensive income	414				414
Deferred stock compensation	(2,087)		(7,014)	D	(9,101)
Retained earnings	282,947		(24,200)	A	258,747
	828,213	7,882			804,013
Total Liabilities and Stockholders' Equity	\$ 1,182,838	\$ 7,882			\$ 1,160,271

LATTICE SEMICONDUCTOR CORPORATION
 UNAUDITED PRO FORMA CONDENSED CONSOLIDATED STATEMENT OF OPERATIONS
 FOR THE YEAR ENDED December 31, 2000 - Revised
 (in thousands, except per share data)

	<u>Lattice</u>	<u>Agere FPGA</u>	<u>Pro Forma Adjustments</u>		<u>Pro Forma Combined</u>
Revenue	\$ 567,759	\$ 142,200			\$ 709,959
Cost of products sold	217,830	72,800			290,630
Gross margin	349,929	69,400			419,329
Operating Expenses:					
Research and development	77,057	10,100			87,157
Selling, general and administrative	81,082	7,810			88,892
Amortization of intangible assets(1)	81,873		18,347	A,D	100,220
	<u>240,012</u>	<u>17,910</u>			<u>276,269</u>
Income from operations	109,917	51,490			143,060
Gain on foundry investment	149,960				149,960
Other income (expense)	2,194		(3,900)	B	(1,706)
Pre-tax income	262,071	51,490			291,314
Provision for income taxes	94,184		11,112	C	105,296
Net income	<u>\$ 167,887</u>	<u>\$ 51,490</u>			<u>\$ 186,018</u>
Basic earnings per share	<u>\$ 1.65</u>				<u>\$ 1.83</u>
Diluted earnings per share	<u>\$ 1.47</u>				<u>\$ 1.62</u>
Shares used in computing basic earnings per share	<u>101,716</u>				<u>101,716</u>
Shares used in computing diluted earnings per share	<u>120,321</u>		414	D	<u>120,735</u>

(1) Pro Forma adjustment includes \$1,754 of deferred stock compensation expense attributable to Research and Development activities.

The accompanying notes are an integral part of these unaudited pro forma condensed consolidated financial statements.

LATTICE SEMICONDUCTOR CORPORATION
 UNAUDITED PRO FORMA CONDENSED CONSOLIDATED STATEMENT OF OPERATIONS
 FOR THE NINE MONTHS ENDED September 30, 2001 -Revised
 (in thousands, except per share data)

	<u>Lattice</u>	<u>Agere FPGA</u>	<u>Pro Forma Adjustments</u>		<u>Pro Forma Combined</u>
Revenue	\$ 243,218	\$ 57,000	\$		\$ 300,218
Cost of products sold	91,676	40,500			132,176
Gross margin	151,542	16,500			168,042

Operating expenses:					
Research and development	54,261	12,500			66,761
Selling, general and administrative	42,064	3,773			45,837
Amortization of intangible assets(1)	63,024		12,648	A,D	75,672
	<u>159,349</u>	<u>16,273</u>			<u>188,270</u>
(Loss) income from operations	(7,807)	227			(20,228)
Loss on foundry investment	(152,795)				(152,795)
Other income (expense)	4,737		(2,925)	B	1,812
Pre-tax (loss) income	(155,865)	227			(171,211)
Benefit for income taxes	(58,863)		(5,831)	C	(64,694)
Net (loss) income	<u>\$ (97,002)</u>	<u>\$ 227</u>			<u>\$ (106,517)</u>
Basic loss per share	<u>\$ (0.89)</u>				<u>\$ (.98)</u>
Diluted loss per share	<u>\$ (0.89)</u>				<u>\$ (.98)</u>
Shares used in computing basic loss per share	<u>108,635</u>				<u>108,635</u>
Shares used in computing diluted loss per share	<u>108,635</u>				<u>108,635</u>

(1) Includes \$1,651 of deferred stock compensation expense (\$336 for Lattice and \$1,315 as part of the Pro Forma Adjustment) for the nine months ended September 30, 2001 attributable to Research and Development activities.

The accompanying notes are an integral part of these unaudited pro forma condensed consolidated financial statements.

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LATTICE SEMICONDUCTOR CORPORATION
UNAUDITED NOTES TO PRO FORMA CONDENSED CONSOLIDATED
FINANCIAL STATEMENTS

This Current Report on Form 8-K/A contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934 and other risks detailed in our Annual Report on Form 10-K for the year ended December 31, 2001 and other reports filed with the Securities Exchange Commission from time to time. Actual results could differ materially from those projected in these forward-looking statements as a result of the risks described above as well as other risk factors set forth in our periodic reports both previously and hereafter filed with the Securities Exchange Commission.

As discussed in Note 2 to the audited financial statements included elsewhere in this report, the pro forma financial statements have been revised to include an allocation of expenses related to Agere's global sales force.

Note 1. Basis of Presentation

On January 18, 2002, Lattice Semiconductor Corporation ("Lattice") completed the acquisition of the FPGA business ("Agere FPGA") of Agere Systems Inc. ("Agere") for \$250 million, in cash. The transaction was completed pursuant to an Asset Purchase Agreement dated as of December 7, 2001 between Lattice and Agere. The components of purchase price are as follows (in millions):

Cash	\$	250.0
Estimated direct acquisition costs		<u>6.3</u>
Total	\$	<u>256.3</u>

In accordance with Financial Accounting Standard (SFAS) No. 141, "Business Combinations," the total purchase price was allocated to the estimated fair value of assets acquired and liabilities assumed. In estimating the fair value of the assets acquired, management considered various factors including an appraisal. The purchase price allocation is subject to further refinement and change over the current quarters. We are in the process of completing integration plans related to Agere FPGA, and accordingly, the amounts recorded are based on our current estimates of these costs. The allocation of purchase price is discussed further in Note 2. The pro forma unaudited condensed consolidated statements of operations exclude the one time charge for IPR&D (Note 2) and are presented using our audited condensed consolidated statement of operations for the year ended December 31, 2000 and our unaudited condensed consolidated statement of operations for the nine months ended September 30, 2001 with Agere FPGA's unaudited statements of Net Sales, Cost of Sales and Direct Operating Expenses for the twelve months ended December 31, 2000 and for the nine months ended September 30, 2001 assuming the transaction occurred on January 1, 2000. The pro forma unaudited condensed consolidated balance sheet gives effect to the acquisition as if the transaction had taken place on September 30, 2001 and combines our unaudited September 30, 2001 condensed consolidated balance sheet amounts with Agere FPGA's audited Statement of Assets to be Sold as of September 30, 2001. For financial reporting purposes, we report on 13 or 14 week quarters with years ended December 30, 2000 and December 29, 2001, respectively. There were no transactions between Lattice and Agere FPGA during the periods

presented. There are no significant differences between the accounting policies of Lattice and Agere FPGA. The pro forma unaudited condensed consolidated financial statements should be read in conjunction with the consolidated financial statements and notes thereto of Lattice, which were previously reported in our Annual Report on Form 10-K for the year ended December 31, 2000 and our Quarterly Report on Form 10-Q for the quarter ended September 30, 2001, on file with the Securities and Exchange Commission, and with the financial statements and notes thereto of Agere FPGA included elsewhere in this Form 8-K/A. These pro forma statements are based on such consolidated financial statements after giving effect to the transaction under the purchase method of accounting and the assumptions and adjustments described below. The pro forma information does not purport to be indicative of the results which would have been reported if the purchase had been in effect for the periods presented or which may result in the future.

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LATTICE SEMICONDUCTOR CORPORATION
UNAUDITED NOTES TO PRO FORMA CONDENSED CONSOLIDATED
FINANCIAL STATEMENTS—continued

Note 2. Pro Forma Adjustments

The pro forma adjustments are based on a preliminary allocation of the purchase price to assets acquired and liabilities assumed. This allocation is subject to refinement and change over the current quarters. In performing this allocation, management considered various factors including an appraisal.

(A) Acquisition of Agere FPGA.

We completed the acquisition of Agere FPGA on January 18, 2002 for \$250 million in cash. Additionally, we paid approximately \$6.3 million in estimated direct acquisition costs. The total purchase price was allocated as follows (in millions):

Excess of purchase price over net assets acquired	\$	142.0
Current technology		63.3
In-process research and development		24.2
Fair value of non-compete agreement		13.8
Licensed technology		10.2
Inventory		2.6
Backlog		1.6
Property, plant and equipment		.2
Accrued liabilities		(1.6)
Total	\$	256.3

There were no significant exit costs incurred or accrued in connection with this transaction.

Inventory was adjusted based upon different disposition plans of certain FPGA products as part of our product offerings.

In-Process Research and Development (“IPR&D”)

IPR&D consists of those products that are not yet proven to be technologically feasible but have been developed to a point where there is value associated with them in relation to potential future revenue. Because technological feasibility was not yet proven and no alternative future uses are believed to exist for the in-process technologies, the assigned value was expensed immediately upon the closing date of the acquisition.

The preliminary value of \$24.2 million assigned to acquired IPR&D was determined by identifying research projects in areas for which technological feasibility has not been established and there is no alternative future use. The fair value of acquired IPR&D includes revisions to the ORCA 4, ORCA 5, FPSC and later generation FPGA products. The value was determined by an income approach where fair value is the present value of projected free cash flows that will be generated by the products incorporating the acquired technologies under development, assuming they will be successfully completed. The estimated net free cash flows generated by the products over 6-7 year periods were discounted at rates ranging from 23 to 25 percent in relation to the stage of completion and the technical risks associated with achieving technological feasibility. The net cash flows for such projects were based on management’s estimates of revenue, expenses and asset requirements.

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LATTICE SEMICONDUCTOR CORPORATION
UNAUDITED NOTES TO PRO FORMA CONDENSED CONSOLIDATED
FINANCIAL STATEMENTS—continued

All of these projects have completion risks related to silicon functionality, architecture performance, process technology availability, packaging technology, continued availability of key technical personnel, product reliability and availability of software support. To the extent that estimated completion dates are not met, the risk of competitors’ product introductions is greater and revenue opportunity may be permanently lost. There has been no material change in the schedule or estimated costs of these projects.

Useful lives of intangible assets

The current and licensed technology has an estimated weighted average useful life of approximately 7 years, and the non-compete agreement’s estimated useful life is approximately 3 years, resulting in a weighted average useful life of approximately 6.3 years. In accordance with SFAS No. 142,

“Goodwill and Other Intangible Assets,” the excess of purchase price over net assets acquired, or Goodwill, will be subject to an annual impairment test and will not be amortized.

(B) Adjustment to reflect the reversal of interest income on the pro forma adjustment to cash resulting from the acquisition. The assumed interest rate was 1.5% which is based upon the current estimated rate of return on our short-term investments.

(C) Adjustment to reflect the tax effect of the pro forma adjustments at our effective rate during the period presented.

(D) Adjustment to stockholders’ equity and amortization expense to record the in-the-money portion of employee stock options issued to former Agere FPGA employees at the time of the acquisition in the amount of approximately \$7 million, attributable to research and development expense, which is being amortized over four years on a straight-line basis using our December 31, 1999 closing stock price as the “grant price.”

Note 3. Pro Forma Earnings (Loss) Per Share

Basic pro forma income (loss) per share was calculated based on shares of our Common Stock outstanding at December 31, 2000 and September 30, 2001. Diluted earnings per share at December 31, 2000 include the addition of common stock equivalents related to stock options and warrants outstanding at that time plus stock options issued to new employees from the Agere FPGA acquisition. In addition diluted shares outstanding at December 31, 2000 includes 12.5 million shares issuable on the assumed conversion of our \$260 million convertible subordinated notes and diluted earnings per share at December 31, 2000 is adjusted to exclude interest expense and debt issuance cost amortization (net of tax) of \$8.3 million and \$1.2 million, respectively. Diluted shares outstanding and earnings per diluted share at September 30, 2001 are the same as the basic shares outstanding and basic loss per share because the addition of common stock equivalents and convertible subordinated notes would be anti-dilutive.

(C) Exhibits.

23.1 Consent of PricewaterhouseCoopers LLP, Independent Accountants

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SIGNATURE

Pursuant to the requirements of the Securities Exchange Act of 1934, the Registrant has duly caused this report to be signed on its behalf by the undersigned hereunto duly authorized.

LATTICE SEMICONDUCTOR CORPORATION

Date: December 19, 2002

By: /s/ STEPHEN A. SKAGGS

Name: STEPHEN A. SKAGGS

Title: Chief Financial Officer

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Consent of Independent Accountants

We hereby consent to the incorporation by reference in the Registration Statements on Form S-8 (No. 33-33933, No. 33-35259, No. 33-38521, No. 33-76358, No. 33-51232, No. 33-69496, No. 333-15737, No. 333-40031, No. 333-59990, No. 333-69467, No. 333-81035, No. 333-67274 and No. 333-99247) and the Registration Statements on Form S-3 (No. 333-15741, No. 333-40043, No. 333-69469, No. 333-93285, No. 333-93289, No. 333-50192, No. 333-59992, No. 333-88128 and No. 333-99249) of Lattice Semiconductor Corporation of our report dated March 7, 2002, except as to the matter described in Note 2, as to which the date is November 21, 2002, relating to the financial statements of the FPGA business of Agere Systems Inc. included in this Form 8-K/A.

/s/ PRICEWATERHOUSECOOPERS LLP

Florham Park, New Jersey
December 17, 2002
