



Lattice Enhances Radiant Design Software with Expanded Functional Safety Capabilities

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– Lattice Radiant integrates latest version of Synopsys Synplify with Triple Modular Redundancy (TMR) to create advanced design automation flow solution –

HILLSBORO, Ore.--(BUSINESS WIRE)--Mar. 25, 2024-- [Lattice Semiconductor](#) (NASDAQ: LSCC), the low power programmable leader, today announced the latest release of its award-winning Lattice Radiant® design software, featuring expanded functional safety and reliability capabilities. Now featuring integration with the latest Synopsys Synplify® FPGA synthesis tool with TMR, Lattice Radiant offers an advanced design automation flow solution that enables designers to more easily develop Lattice FPGA-based applications with the robust functional safety protections, high reliability, and dependable operation required for the Industrial, Automotive, and Avionics markets.

Establishing protocols for functional safety and error mitigation compliant with industry standards, namely DO-254, IEC 61508, and ISO 26262, is integral to developing and validating highly reliable and safety-critical designs. Integrating Lattice Radiant with Synopsys Synplify Triple Modular Redundancy (TMR), automates the required industry practices, specifically addressing the mitigation of soft errors such as Single Event Upsets.

“At Lattice, we are committed to delivering continued innovation in our design tools that make them easy-to-use, reliable, and secure as devices advance to higher logic densities, requiring higher functional safety and reliability,” said Dan Mansur, Corporate Vice President of Product Marketing at Lattice Semiconductor. “The latest Radiant software with Synopsys TMR capabilities will provide automated synthesis protocol with enhanced efficiency and reliability, enabling designers to further explore the robustness of our low power, small form factor FPGAs.”

The latest Lattice Radiant release includes:

- Safety Critical Block-Based Design Flow.
- Interactive Tcl Based Static Timing Analysis enabling faster timing closure.
- Multi-bit error injection for Soft Error testing.

“Automating the FPGA design process with high reliability and functional safety is essential for developing complex designs that meet industry standards requirements for safety-critical applications in industrial, automotive, and avionics markets,” said Tom De Schutter, VP of engineering for the Systems Design Group at Synopsys. “Expanding our collaboration with Lattice helps designers accelerate development of their low power, performance-optimized FPGA-based designs using Synopsys Synplify’s complete FPGA synthesis design flow.”

Supporting Resources

- Learn more about [Lattice Radiant](#).
- Learn more about [Synopsys Synplify](#).

About Lattice Semiconductor

Lattice Semiconductor (NASDAQ: LSCC) is the low power programmable leader. We solve customer problems across the network, from the Edge to the Cloud, in the growing Communications, Computing, Industrial, Automotive, and Consumer markets. Our technology, long-standing relationships, and commitment to world-class support let our customers quickly and easily unleash their innovation to create a smart, secure, and connected world.

For more information about Lattice, please visit www.latticesemi.com. You can also follow us via [LinkedIn](#), [Twitter](#), [Facebook](#), [YouTube](#), [WeChat](#), or [Weibo](#).

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