



New Lattice Radiant 3.0 Design Software Further Enhances Ease of Use to Accelerate FPGA Designs

June 23, 2021

HILLSBORO, Ore.--(BUSINESS WIRE)--Jun. 23, 2021-- [Lattice Semiconductor Corporation](#) (NASDAQ: LSCC), the low power programmable leader, today announced availability of the latest version of its popular software design tool for use with low power Lattice FPGAs, [Lattice Radiant® 3.0](#). The tool supports higher density devices like the new [Lattice CertusPro™-NX](#) family – the latest family based on the [Lattice Nexus™](#) platform – and offers new features that make it faster and easier than ever to develop Lattice FPGA-based designs.

When system developers evaluate hardware platforms, the actual hardware is only a part of their selection criteria. They also evaluate the design software used to configure the hardware for its ease of use and supported features, as those characteristics can have a significant impact on overall system development time and cost.

“As a leading provider of FPGA-based SoM solutions for the industrial and automotive markets, we have decades of experience working with various software tools used in hardware development,” said Antti Lukats, CTO, Trenz Electronic GmbH. “The Lattice Radiant tool has a modern user interface that is highly intuitive and very easy to use, which reduces design complexity and helps us get products to market faster.”

“Lattice Radiant 3.0 design software gives developers an easy-to-follow user experience; the tool leads them through the steps of the development flow, including design creation, importing IP, implementation, bitstream generation, downloading the bitstream onto an FPGA, and debugging,” said Roger Do, Senior Product Line Manager, Software at Lattice Semiconductor. “Developers with little to no experience working with FPGAs can quickly leverage the automated features of Lattice Radiant. For experienced FPGA developers, Lattice Radiant 3.0 allows for more granular control over FPGA settings if specific optimizations are required.”

New feature upgrades available in Radiant 3.0 include:

- The SERDES analysis tools in Radiant 3.0 have been enhanced to accommodate the higher SERDES bandwidths supported by CertusPro-NX devices.
- Improved signal traceability throughout the design flow via the graphical user interface (GUI) to help designers trace a signal between the HDL source to the RTL view, and to the technology view and back again.
- Radiant allows the user to choose between the Lattice Synthesis Engine (LSE) and the Synplify Pro® synthesis engine. In Radiant 3.0, timing constraints and timing analysis are unified across both synthesis engines.
- In Radiant 3.0, timing analysis has been separated from other operations so it can run independently. This dramatically speeds the iterative design process by helping designers evaluate “what-if” scenarios and re-run timing analysis without having to re-run mapping and place-and-route.
- Radiant 3.0 averages a 15 percent reduction in runtime and a 7 percent increase in design performance in comparison to the previous release.

For more information about the Lattice technologies mentioned above, please visit

- www.latticesemi.com/LatticeRadiant
- www.latticesemi.com/CertusPro-NX
- www.latticesemi.com/LatticeNexus

About Lattice Semiconductor

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For more information about Lattice, please visit www.latticesemi.com. You can also follow us via [LinkedIn](#), [Twitter](#), [Facebook](#), [YouTube](#), [WeChat](#), [Weibo](#) or [Youku](#).

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